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Research Article

SELECTIVE TRANSISTOR REDUNDANCY FOR COMBINATIONAL CIRCUITS TO REDUCE FAULTS

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A B S T R A C T

Now a days, CMOS devices are becoming more popular and with fabrication technology reaching nano levels, systems are getting additional vulnerable to producing defects with higher susceptibleness to soft errors. Soft errors are the errors that are caused by high density materials, coupling etc., the existing methods are not perfect in order to reduce the errors with increase in no of transistors. This paper is concentrated on coming with combinatory circuits for soft-error correction with less space overhead. This concept is predicated on generating a random pattern series for testability of faults in a combinational circuit and protects the transistors, whose soft error detection high, this process is continued till the combinational circuit produces the correct output as similar as input. In this paper we are proposing a selective transistor redundancy algorithm which selects the transistor whose probability of failure is high and protects the transistor to reduce errors. This process is continued until a certain area overhead or threshold limit is obtained.

INTRODUCTION

Over past few years, many changes were happened. Many technologies have developed for providing reliable and faster communication among devices. The scaling of CMOS devices also increases in a rapid way, which leads the devices in nanoscale size. These nano scale devices are limited by some features like high device effect rates and susceptible to soft errors and so that the errors that are going to occur in the combinational circuits are also increasing and the present methods are not efficient to reduce the errors. These errors are called as soft errors. Soft error is an error that is occurred whenever an wrong signal or data is encountered. Due to these type of errors the performance of the circuit is reduced. Soft errors or transient errors may occur due to several reasons. Some of them are high energetic materials, coupling and leakage. In a combinational circuit these soft errors may occur for several clock cycles. Due to this occurrence for several clock cycles this leads to transient current pulses. Several transient current pulses can be called occurred by a single event transient at the output.[1]

To protect individual transistors in the combinational circuit. We use selective transistor scaling technique. To protect the transistors of the combinational circuit we use either transistor duplication or asymmetric sizing. The nMOS and pMOS transistors can be sized separately. Transistor duplication is a technique which duplicates the transistors in a circuit.

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This can be done in two ways. One way is to duplicate the entire circuit .The another way is to protect some of the transistors based on the failure rate.

One of the technique that is used for error correction in designing logic circuits is triple modular redundancy. The main idea is to develop three copies of the system. The input is given to the three systems and the output of the three systems is given to voter. The voter selects the correct output from the three systems and gives the correct output. This technique is cost effective. Two reduction techniques that can be used are cluster sharing reduction and dominant value reduction are used to reduce the soft error failure rate.

Triple modular redundancy, is also called triple-mode redundancy, (TMR) is a fault correction form of N-Modular Redundancy, in which three systems performs a method and that output from the three systems are processed by a majority-voting system to produce a particular output. If any one of the three systems fails, the other two systems will correct and corrects the fault.[2]

The TMR can be use in many forms such as software redundancy in the form of N-version Programming, It is mostly found in Fault Tolerant Computer Systems. Some ECC memory uses this technique because it is quicker than Hamming error correction technique. This technique is mostly used in space satellite systems. This method targets the nodes with highest soft error vulnerability.

Some of the drawbacks of the existing system is

- voter a single point failure

- high redundancy costs
- power consumption
- area over head [3]

Proposed Method

The proposed technique performs the fault correction by using a random pattern generator to generate a random pattern of bits that is given to a combinational circuit and checked for the correct output at the end of the combinational circuit and if any of the input got wrong then it is corrected using the STR algorithm. STR means selective transistor redundancy. This can be done using SPICE.[4] STR algorithm is as shown below.

STR Algorithm

Calculate the failure probability of a transistor using the procedure.

$\mathrm{POF_{ij}} = \mathrm{P_{DET_{ij}}} \times \mathrm{P_{HIT_{ij}}}$

Compute $\mathrm{POF_c}$for all transistors using the equation.

$$\mathrm{POF_c} = \sum_{i=0}^{m}\sum_{i=0}^{n} \mathrm{POF_{ij}}$$

Target area = circuit-area+ (circuit-area*overhead)
While($\mathrm{POF_c}$>=TH-1) or (circuit area<target area) then
Pick a transistor whose $\mathrm{POF_{ij}}$is highest and protect it.
Update circuit area.
Update $\mathrm{POF_{ij}}$ of transistors.
Update$\mathrm{POF_c}$.
End while

Let us first identify the Probability of failure of a transistor. Here i is referred for gate and j is referred for transistor .The P_{ij} of the j^{th}transistor of gate i is given by

$$\boldsymbol{P_{ij} = P_{D_{ij}} \times P_{H_{ij}}}$$

where$P_{D_{ij}}$ is the probability of detecting a fault hitting transistor j of gate i at a primary output, and $P_{T_{ij}}$is the probability that transistor j of gate i is hit by a fault.[5]

The greater the transistor width/area is, the greater its hit probability is $P_{H_{ij}}$is computed separately for nMOS and pMOS transistors as they have different drain widths. Let$NW_{ij}$and PW_{ij}be the width of nMOS and pMOS transistors, respectively, and Area be the total circuit area; then, the probability of a transistor j of gate i to be hit by a fault, $P_{H_{ij}}$, is computed using the following

$$\boldsymbol{P_{H_{ij}} = \frac{W_{ij}}{AREA} W_{ij} \in \{NW_{ij}, PW_{ij}\}}$$

$P_{D_{ij}}$depends on two factors:

1. The Probability of input patterns when a fault hits the transistor is propagated to the output of a gate
2. Stuck-at fault observability probability of the gate at one of the primary outputs of a circuit, i.e., observability probability. $P_{D_{ij}}$is calculated by

$$\boldsymbol{P_{D_{ij}} = P_{Excitation_{ij}} \times P_{Prop\ agation_{ij}}}$$ where $P_{Excitation_{ij}}$denotes the probability that the fault is keyed up at gate i output due to a fault hit at transistor j. $P_{Propagation_{ij}}$denotes the probability that an error that is excited at the gate's output is observable at one of the primary outputs. Let S be a set of patterns for which an error that strikes transistor j is propagated to the output of gate i then, $P_{Excitation_{ij}}$is computed as

$\boldsymbol{P_{Exicitation_{ij}} = \sum_{K=1}^{|S|} Prob.S_k}$ where Prob.S_k is the probability of incidence of the kth input model. SPICE tool is used to find the input patterns for which a transistor fault is excited and observed at the gate output.

Similarly, $P_{Propagation_{ij}}$can be computed using the following relation.[6]

$$\boldsymbol{P_{Prop\ agation_{ij}} = \frac{\mathrm{prob}_i}{\mathrm{PC}_i}}$$

Where prob_i defines stuck-at fault detection probability of gate i and PCi is the probability to produce logic value opposite to the fault at the output. Finally, the circuit PC for a single fault is simply the summation of POFs of all transistors n over all gates m of a circuit

$$\mathrm{P_C} = \sum_{i-1}^{m}\sum_{j=1}^{n} \mathrm{P_{ij}}$$

Reliability Evaluation

A novel method to compute the reliability of a circuit at the gate level is proposed in this section. The proposed technique bridges the gap between circuit-level simulations performed at the transistor level using SPICE and gate-level simulations, which could be done using any gate-level simulator. In this realm, we propose the probability of fault injection, which quantifies the probability with which a fault must be injected at the gate level, so that SPICE-level and gate-level simulation results are highly matched.

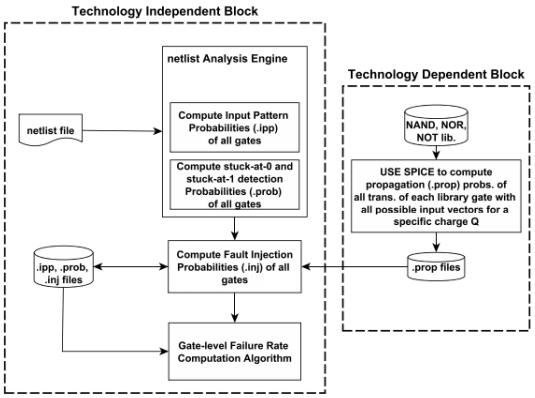

Fig 1 Reliability evaluation framework

The reliability evaluation framework, shown in, consists of two major blocks:

Technology-independent block
Technology-dependent block. [7]

Technology Independent Block

The purpose of the technology-independent block is to analyze a given benchmark circuit to compute three important parameters for all gates:

1. input pattern probability (.ipp),
2. stuck-at detection probability (.prob) and
3. fault injection probability (.inj).

The input patterns visible at each gate input along with their probability of occurrence and stuck at fault detection probabilities are calculated by performing the simulation of

random test vectors using the parallel fault simulator. The fault injection probability denotes the probability with which a fault must be injected at the gate level as a stuck-at fault. These results are stored for later usage.[8]

Technology dependent Block

The technology-dependent part mainly consists of the library gates comprising NAND/NOR gates with changeable input configurations and an inverter. The purpose of this block is to observe the behaviour of different process technologies, this block computes the effect of an induced current of charge (Q) for every transistor of the gate in the library. The input patterns that result in a gate value flip when a transistor is hit are then saved in the propagation (.prop) file. In fact, we can compute and save the behaviour of different technologies against different charge (Q) values, and this has to be done only once.

Now, the fault injection probability of a gate in a circuit can be computed for any process technology. It must be noted that the initial analysis of a circuit has to be done only once. Sections V-A–V-C contain the detailed elaboration of the reliability evaluation framework.[9]

Probability of Fault Injection

The fault injection probabilities of a gate depend on the conditional fault excitation probability ($CFEP_{ij}$) and probability of hit/selection

Then, $CFEP_{ij}$ can be defined as

$$\mathbf{CFEP_{ij}} = \frac{\sum_{k=1}^{|s|} \mathbf{Prob.S_k}}{\mathbf{PC_i}} = \frac{\mathbf{P_{Excitation_{ij}}}}{\mathbf{PC_i}}$$

$CFEP_{ij}$ of any MOS transistor depends on the process technology and the charge of the incident particle. Therefore, in order to get the exact $CFEP_{ij}$ probability for each MOS transistor, transistor-level simulations are performed using SPICE.[10]

Now, the sa0 fault injection probability of gate G_i is computed using the following equation:

$$G_i sa_0 inj.Prob = \sum_{j=1}^{n} (CFEP_{N_{ij}} \times \frac{NW_{ij}}{\sum_{k=1}^{n} NW_{ik}})$$

where n is the total number of nMOS transistors in gate Gi , NW_{ij} is the width of the drain of the jth nMOS transistor, and $CFEP_{Nij}$ is the CFEP due to a fault hit at the jth nMOS transistor of gate i.

Similarly, the sa1 fault injection probability of gate G_i is computed as follows.

$$G_i sa_1 inj.Prob = \sum_{j=1}^{p} (CFEP_{p_{ij}} \times \frac{PW_{ij}}{\sum_{k=1}^{n} PW_{ik}})$$

where p is the total number of pMOS transistors in gate G_i ,PW_{ij} is the width of the drain of the jth pMOS transistor, and $CFEP_{Pij}$ is the CFEP due to a fault hit at the jth pMOS transistor of gate i.

SIMULATION RESULTS

The faults can be corrected by using STR algorithm by first designing a random pattern generator. The random pattern generator generates a random input pattern that is given to a combinational circuit and it is checked for the output. If the output is same as input then it is called an errorless output. The combinational circuit that is used in this paper is a two input AND gate and the results are shown below.

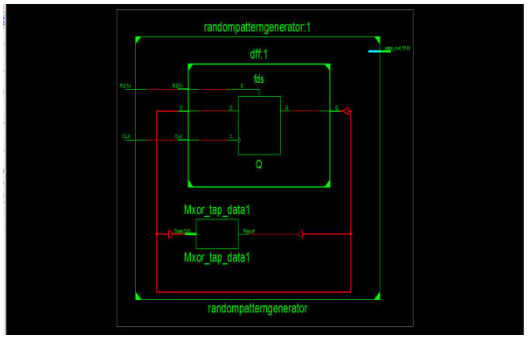

Fig2(a) random pattern generator

This random pattern generates a random input pattern that is to be given two input AND gate and the results that is compared with input and output are as shown below:

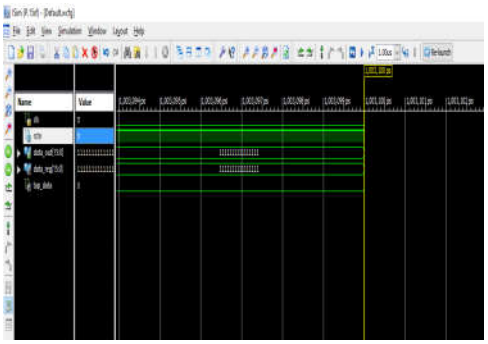

Fig 2(b) comparison of input and output patterns for correction of faults

The analysis of the two input AND gate can be done with the help of the graphs like frequency vs time, eye diagram etc., an are shown below

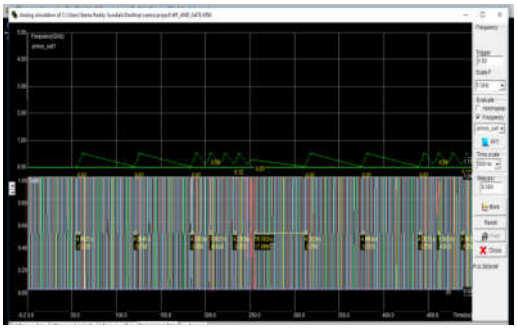

Fig:2(c) frequency vs time

The above fig shows the analysis of frequency and time and the ripples in the graph shows the transistors which causes the errors.

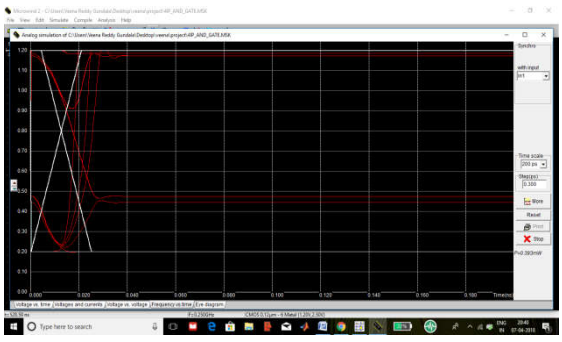

Fig 2(d) eye diagram

The eye diagram represents the inter symbol interference of the circuit.

The power consumed of the circuit is can be given by

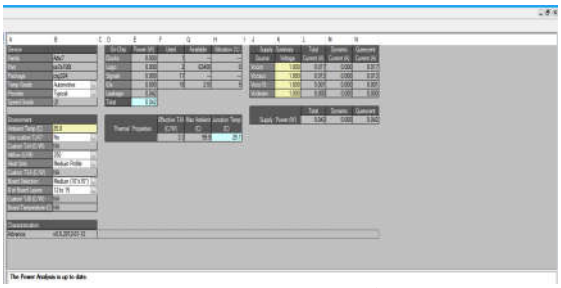

Fig 2(e) power consumption

CONCLUSION

In this paper, the proposed method was implemented which reduces the faults by reducing the power consumption. The important factor in CMOS technology is area. By using this technique the area consumption also reduces than the existing methods like triple modular redundancy. Better reliability results are also achieved in comparison to TMR with lower area overhead. Unlike TMR, which has an area overhead of at least three times the area overhead of the original circuit, the area overhead of the proposed technique varies depending on the reliability of the original circuit. Hence as the area reduced then the cost of the system also decreases.

The following are the advantages that will occur by using the proposed method.

- Reduces the faults in a higher rate which leads to provide high accuracy.
- Area required also reduces.
- Cost of the system decreases.
- The reliability of the system increases

The proposed architecture can be extended to sequential circuits which have memory elements in them.

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