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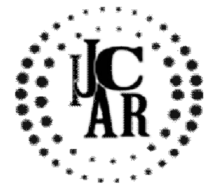

Research Article

3D-TCAD SIMULATION STUDY OF PROCESS VARIATIONS ON V_t IN 130NM GATE LENGTH MOSFET

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ABSTRACT

This paper investigates the effect of process variations on threshold voltage (V_t) in 130nm gate length MOSFET by performing extensive 3D TCAD simulations. Sensitivity of V_t on channel doping, gate oxide time and gate oxide temperature are studied. It's found that $V_t$is sensitive to channel doping and gate oxide thickness in the right manner which refers to equation for calculating V_t.

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INTRODUCTION

MOSFET, in conjunction with other circuit elements, is used extensively in digital circuit applications where thousands of devices can be fabricated in a single integrated circuit. Without doubt, MOSFET is the core of integrated circuit design at the present time.

A metal-oxide-semiconductor field-effect-transistor (MOSFET) is based on the modulation of charge concentration by a MOS capacitance between a body electrode and a gate electrode located above the body and insulated from all other device regions by a gate dielectric layer which in the case of a MOSFET is an oxide, such as silicon dioxide (SiO_2). The MOSFET includes two additional terminals (source and drain), each connected to individual highly doped regions that are separated by the body region. These regions can be either p or n type. In this document NMOS transistor is chosen for analysing the process variation on threshold voltage (V_t).

Threshold voltage was defined as the applied gate voltage required to form inversion layer between oxide and body. The formation of the inversion layer allows the flow of electrons through the gate-source junction. The threshold inversion point, in turn, is defined as the condition when the surface potential is $\emptyset_s = 2\emptyset_{fp}$ in p-type semiconductor. The threshold voltage will be derived in terms of the electrical and geometrical properties of the MOS capacitor.

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Threshold voltage expression:

$$V_t = V_{t0} + \gamma\left(\sqrt{\emptyset_s + V_{sb}} - \sqrt{\emptyset_s}\right) \quad (1)$$

Which γisbody effect coefficient and defined as follow:

$$\gamma = \frac{\sqrt{2q\varepsilon_{si}N_A}}{C_{ox}}$$

with

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

V_{t0} is the threshold voltage when the source is at the body potential.

$$V_{t0} = \frac{|Q'_{SD}(max)|}{C_{ox}} + V_{FB} + 2\emptyset_{fp} \quad (2)$$

Some parameters related to equation (1) and (2):
$\emptyset_S$: surface potential
N_A: doping level in the channel
ε_{ox}, ε_{Si}: permittivity of SiO_2 and Si
t_{ox}:thickness of oxide layer
Q'_{SD}: oxide charge
V_{FB}:flat-band voltage
$\emptyset_{fp}$:difference (in volt) between E_{Fi} and E_F
From the equation, we can see that: for a given semiconductor material, oxide material andgate material, the threshold voltage is a function of semiconductor doping, oxide charge and oxide thickness.

Simulation Environment

TCAD simulator from Silvaco is used to perform all the simulations. This simulator has many facilities and the following modules are used in this study.

- ATHENA: this tool performsstructure initialization and manipulation and provides basic deposition and etch facility
- ATLAS: is used in conjunction with the ATHENA process simulator. ATLAS provides general capabilities for 2D and 3D simulation of semiconductor devices, which predicts the electrical characteristics associated with specified bias condition.
- TonyPlot: is a graphical post processing tool for use with all Silvacosimulator.
- TonyPlot3D: is a 3Dgraphics viewer, capable of displaying data generated from 3D process and device simulator
- DevEdit: is a device structure editor. It can be used to generate a new mesh on an existing structure, modify a device or create a devide from scratch.

3-D device structure of NMOS transistor generated from ATHENA and DevEdit is shown in Figure 1. Figure 2 show 2D structure which depicts the cross section of NMOS. Figure 3 show the schematic of a typically NMOS transistor.

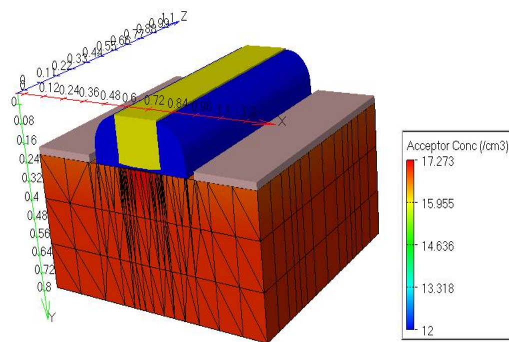

Figure 1 3D structure of NMOS transistor

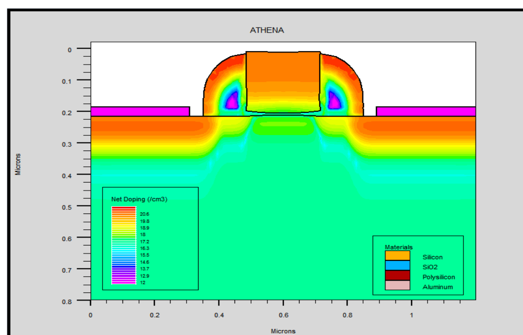

Figure 2 2D structure of NMOS transistor

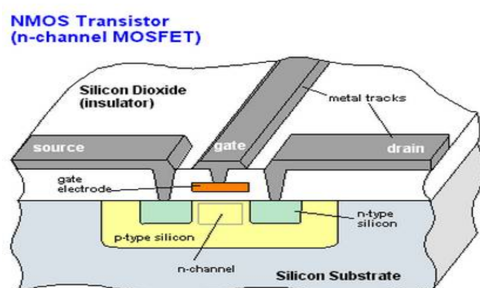

Figure 3 Schematic of 2DnMOS structure

In this document, some process parameters will be lightly changed to show the influence to threshold voltage. As mentioned, threshold voltage is the gate voltage where an inversion layer forms at the interface between the insulating layer (oxide) and the substrate (body) of the transistor. Equation (1) and (2) show that threshold voltage depends on some process parameters such as channel doping and oxide thickness, as listed in table 1. We use TCAD simulator tools as mentioned to check the influence of channel doping, oxide thickness on Vt.

Table 1 Process parameters affect to threshold voltage

Process parameters	Nominal value	Range of value
Channel doping	4E17	1.5E15 → 4E18
Gate oxide time	11 min	5 → 14
Gate oxide temp	875	750→975

RESULTS AND DISCUSSION

Variation in channel doping

Figure 4 show the variation of Vt versus channel doping (N_A). It can be observed from fig. 4 that Vt increases when channel doping increases in concentration, but the increasing steps is not steady.

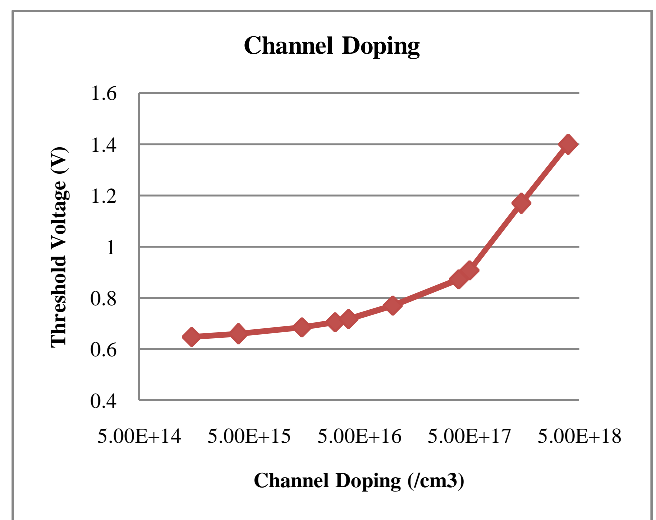

Figure 4 Variation of V_t against channel doping

From equation(1), we see that threshold voltage is proportionalto body effect coefficient, so that it is also proportional to channel doping (N_A), if channel doping increases in concentration, V_t will increase as well. Simulation results in TCAD tools are reasonable for dependence of V_t on channel doping (N_A) if compared to theory on V_t.

Variation in Gate Oxide Time

Figure 5 show the variation of V_t versus gate oxide time. It can be observed from fig.5 that Vt increases with gate oxide time but the increasing steps is not steady. Refer to the formula for calculation of body effect coefficient, when oxide thickness increases, body effect coefficient will increase, so that the threshold voltage (V_t) also increases.

When the time for creating gate oxide layer increases, we derive thicker gate oxide layer, that means gate oxide time is proportional to V_t. Simulation results in TCAD tools is reasonable for dependence of V_t on oxide gate time.

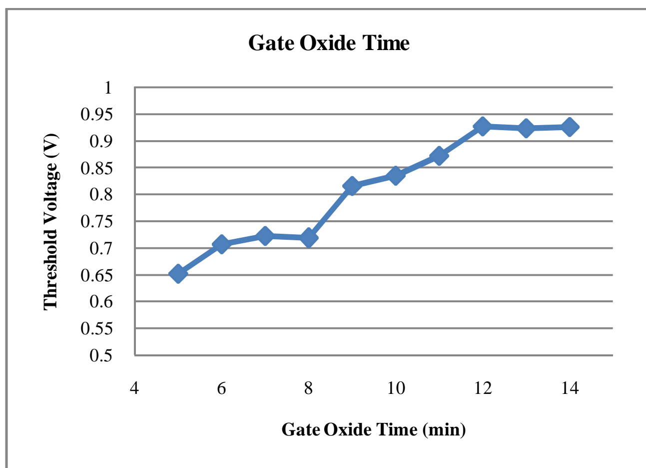

Figure 5 Variation of gate oxide time on V_t

Variation in Gate Oxide Temperature

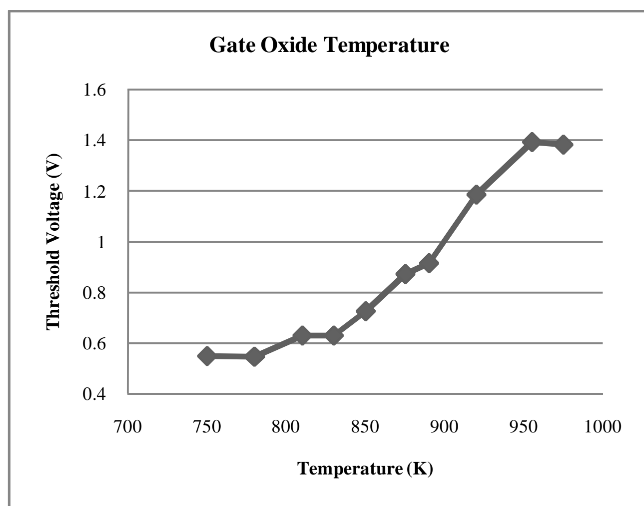

Figure 6 Variation of gate oxide temperature on Vt

Figure 6 show the variation of V_t versus gate oxide temperature. It can be observed from fig.6 that Vt increases with gate oxide temperaturebut the increasing steps is not steady.

Refer to the formula for calculation of body effect coefficient, when oxide thickness increases, body effect coefficient will increase, so that the threshold voltage (V_t) also increases. When the temperature for creating gate oxide layer increases, we derive thicker gate oxide layer, that means gate oxide temperature is proportional to V_t. Simulation results in TCAD tools is reasonable for dependence of V_t on oxide gate temperature.

CONCLUSIONS

Three process parameters – channel doping, gate oxide time, gate oxide temperature were considered in this study to find their variational impact on threshold voltage (Vt). The simulation results show that the impact of three process parameters on Vt is reasonably compared with theoretic equations.

Acknowledgment

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